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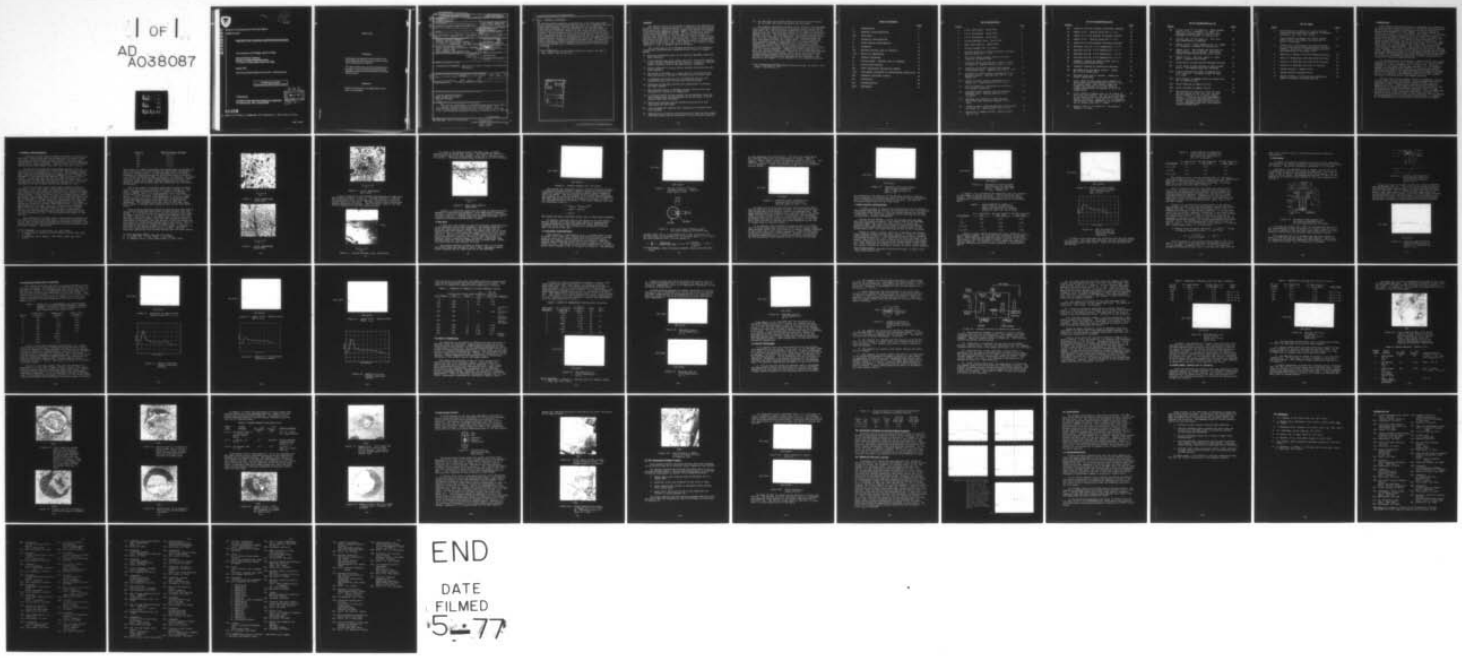

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PROTECTIVE COAXIAL SWITCHING DEVICES

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COAXIAL SWITCHING DEVICE
NEMP PROTECTIVE DEVICE
NIOBIUM DIOXIDE

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

The use and performance of NbO/NbO_2 chips supplied by ECOM in a coaxial switching device has been investigated. The material does exhibit switching with a delay time of less than 1 ns. The threshold switching voltage is typically 100 to 300 V.

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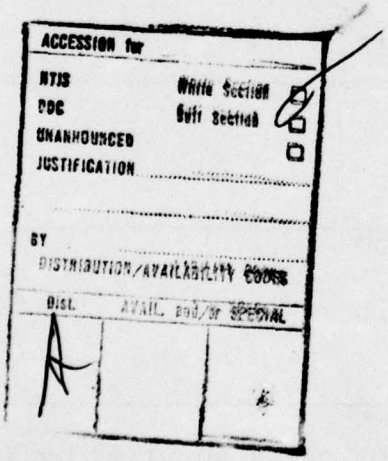
20. ABSTRACT (CONTINUED)

A manufacturable packaging configuration with evaporated small area contacts has been developed and fifty (50) completed devices have been supplied. Step by step details of all pertinent fabrication procedures, from selection of as received chips to final mounting and wire bonding of the completed unit are described. Device stability for a range of pulse lengths has also been investigated and is discussed in some detail. The electrical parameters of the as supplied chips do not however meet the specifications listed in the Technical Guidelines DAAB07-76-Q-1335 which require a threshold switching voltage <100. In addition, device degradation with repeated pulsing is observable even for 3 ns pulse widths and is markedly accelerated for larger pulse widths.*

* For a definition of threshold switching voltage, as used in this report, see Section XIV.



SUMMARY

The present study was initiated to determine the feasibility of using niobium dioxide material in a threshold switching device which serves as a means of circuit protection against the effects of Nuclear Electromagnetic Pulses (NEMP). According to the Technical Guidelines DAAB07-76-Q-1335, the device must have sufficiently high impedance in the off state to ensure minimum insertion loss (less than 0.4 dB at 200 MHz); while in the on state the device voltage should never exceed 100 V with a corresponding delay time of less than 1 ns. The niobium dioxide material was supplied by ECOM in the form of thin layers ~ 10 μ thick on a NbO substrate ~ 3 mm in diameter and 0.6 mm thick.

The investigation has proceeded according to the following (essentially chronological) steps which are listed in summary below:

1) Material characterization of the supplied NbO/NbO_2 chips has been completed.

2) A test system with cable pulser and 75 ps resolution sampling scope has been assembled and calibrated. A system to measure device insertion loss at 480 MHz has been assembled.

3) System response to various device package configurations has been measured.

4) Switching of NbO/NbO_2 in a point contact configuration has been evaluated to provide a reference point to prior work.

5) A packaging configuration for the NbO/NbO_2 devices with evaporated small area contacts has been developed.

6) Switching of NbO/NbO_2 devices with evaporated Al contacts has been studied.

7) The characteristics of NbO/NbO_2 coaxial devices have been measured as a function of temperature.

8) A sputtered Nb/Au contact system for the NbO/NbO_2 chips has been prepared and the performance characteristics of these devices have been evaluated.

9) Twenty-four mounted coaxial switching devices have been fabricated and delivered.

10) Failure modes for samples with evaporated Al contacts have been studied.

11) Samples with no foreign contact materials (back-to-back chips) have been pulsed and failure modes in these devices observed.

12) An additional 26 mounted coaxial switching devices (making 50 in total) have been fabricated and delivered.

The primary conclusions to date are as follows: The NbO/NbO_2 chips supplied by ECOM do exhibit switching with a delay time of less than 1 ns. The electrical parameters of these chips do not however meet the specifications listed in the Technical Guidelines DAAB07-76-Q-1335. The threshold switching voltage* is typically 100-300 V and not <100 V as specified. Switching characteristics and off state resistance are highly variable between chips and even from place to place on a single chip. Device degradation with repeated pulsing is observable for 3 ns pulse width and degradation is markedly accelerated for larger pulse widths. Samples subjected to long (50 ns) pulses or extensive pulsing (thousands of 3 ns pulses) exhibit deep channels through the NbO_2 layer to the NbO substrate. Samples with less severe pulsing show less physical damage, but deterioration is sometimes observed in device off state resistance. There is no clear correlation between physical damage and device off state resistance. The switching characteristics and degradation with pulsing of the devices do not appear to be a function of the electrode material.

* For a definition of threshold switching voltage, as used in this report, see Section XIV.

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I. INTRODUCTION

The present study was initiated to determine the feasibility of using niobium dioxide material in a threshold switching device which serves as a means of protection against the effects of Nuclear Electromagnetic Pulses (NEMP). To prevent damage to sensitive circuitry, e.g., a receiver input stage, it is necessary to provide a voltage responsive device to shunt the incoming pulse to ground before reaching any such circuit elements. The device will normally be in a state of high impedance so as to cause minimal insertion loss in this normal or "OFF" mode. Upon being subjected to NEMP, the device must switch, with a minimum delay time, to a low impedance "ON" state, thus shunting and reflecting the incoming pulse. The reverse transition to the high impedance "OFF" state is effected by the end of the incoming pulse. Switching characteristics should be reproducible over the operating temperature range of the equipment and the device should be capable of withstanding many rapid switching cycles under the full range of environmental conditions without significant alteration of operating characteristics.

For the purpose of this contract, ECOM furnished the niobium dioxide material in the form of thin layers ~ 10 μ thick on NbO substrates ~ 3 mm in diameter and ~ 0.6 mm thick. The work covered in this report had two main thrusts: (1) to determine whether the niobium dioxide material as supplied did exhibit switching and whether its characteristics fulfilled the requirements as set forth in the Technical Guidelines DAAB07-76-Q-1335, and (2) to formulate a manufacturable housing for the coaxial protective switching device with bonded contacts.

The main text of this report follows in essentially chronological order the work procedures, tests performed and results achieved in the evaluation of the niobium dioxide chips as supplied by ECOM. A preliminary statement of manufacturing feasibility is also given based on the experience gained in the fabrication of 50 niobium dioxide switching devices already delivered under terms of the work agreement. This includes step by step details of all pertinent fabrication procedures from selection of as received chips to final mounting and wire bonding of the completed unit in microwave diode packages. A summary of accomplishments to date is given at the end of the report.

II. MATERIAL CHARACTERIZATION

A study of the NbO chips as grown by Yeshiva University has been made. These chips were melt-grown single crystals of NbO that were cleaved and then surface oxidized. The chips were approximately 3 mm in diameter and 0.6 mm thick with substantial variations in these dimensions. Samples were from five different batches whose batch numbers were 101, 102, 104, 105, and 110.

Verification was made by x-ray powder patterns that the crystal body of the chips was actually NbO with a cubic structure and x-ray lattice parameter of $a = 4.211 \pm .005$ Å (sample #101). This value is in good agreement with Bowman et al,[1] Brauer and Morawietz,[2] and Anderson and Magneli[3] who all found $4.2105 \pm .004$ Å. It was also verified by x-ray back reflection on a cleavage face of NbO that the cleavage face is {100}. This might be expected since the NbO structure is related to,[1,3] but not identical with that of NaCl, which also cleaves on {100}.

All of the single crystal chips were cleaved at Yeshiva University so that the large, active faces for the devices were {100} NbO faces. The chips, as cleaved but not further polished, were surface oxidized at Yeshiva to give a thin layer of a higher niobium oxide. It was verified by an x-ray powder pattern that this layer was actually NbO_2, at least for a chip from Batch #105. The recipe used by Yeshiva University for making this NbO_2 layer was as follows: 2 g of NbO chips (an average chip has a mass of about 3×10^{-2} g) plus 8 g of NbO_2 powder plus 0.1 g of Nb_2O_5 powder was placed in a sealed, fused quartz tube 1.4 cm diam. and approximately 10 cm long. The air in the tube was evacuated before sealing. The tube was heated to 800 °C for 24 hours, 1000 °C for 2 hours, and 900 °C for 22 hours, consecutively. The tube was then removed abruptly from the furnace and cooled to room temperature in air. All five batches were done in this same way.

The thickness of the NbO_2 layer so produced was measured for each batch by cleaving the NbO along a (010) plane perpendicular to its (100) surface and then studying the fracture surface. The results using an optical microscope and a scanning electron microscope were similar. These were:

1. A.L. Bowman, et al Acta Cryst. 21, 843 (1966).
2. G. Braver and H. Morawietz, Zeit. anorg. allgem. Chem. 317, 13 (1962).
3. G. Anderson and A. Magneli, Acta Chem. Scand. 11, 1065 (1957).

Batch #	NbO_2 Thickness, Microns
101	10 ± 2
102	11 ± 2
104	11 ± 2
105	11 ± 2
110	9 ± 2

Some areas on a sample from Batch #105 showed NbO_2 thicknesses of up to 20 microns in a region where the NbO surface possessed a series of cleavage steps. It was concluded that it might be necessary to carefully polish the NbO surfaces before oxidation if a uniform thickness of NbO_2 is desired. In addition, the gross flatness of the "as cleaved" chips supplied was variable. Some chips had ridges and valleys thereby preventing good contact between a mask and the NbO_2 layer for evaporation or sputtering of contacts.

The x-ray study of some NbO_2 power made from Nb and Nb_2O_5 in the tri-arc furnace at Yeshiva University on August 1, 1974 gave a tetragonal structure with a = 13.692 ± .003 Å and c = 5.983 ± .003 Å. This is in good agreement with literature values[4,5,6] which can be represented by: a_o = 13.70 ± 0.02 Å and c_o = 5.980 ± .005 Å at room temperature. The x-ray study of the NbO_2 surface layer on the NbO chips (from Batch #105) showed the same tetragonal structure with the same lattice parameters. The orientation of the c-axis of this NbO_2 layer with respect to the NbO (100) substrate has not yet been determined.

Some scanning electron microscope pictures have been made of as received cleaved NbO chips after the NbO_2 surface layer was formed. A view looking down on to the top surface of the chips is shown in Figures 1, 2, 3 for samples from Batches #102, #104, and #105. The grain size of the NbO_2 layer is about 3 microns. The magnification is 2000X. Note that the surface structure of each batch is different, that the surface is far from smooth and that there are vacant pores between some of the grains. This is particularly true of the sample from Batch #104. If the top electrode of the device is about 5 x 10^{-3} inches in diameter, it will cover about 2000 different grains of NbO_2. Thus the electrical properties will be some average over all these grains.

4. B.O. Marinder, Arkiv. Kemi 19, 435 (1963).
5. N. Terao, Jap. J. Appl. Phys. 2, 565 (1963).
6. A. Magneli, et al., Acta Chem. Scand. 9, 1402 (1955).

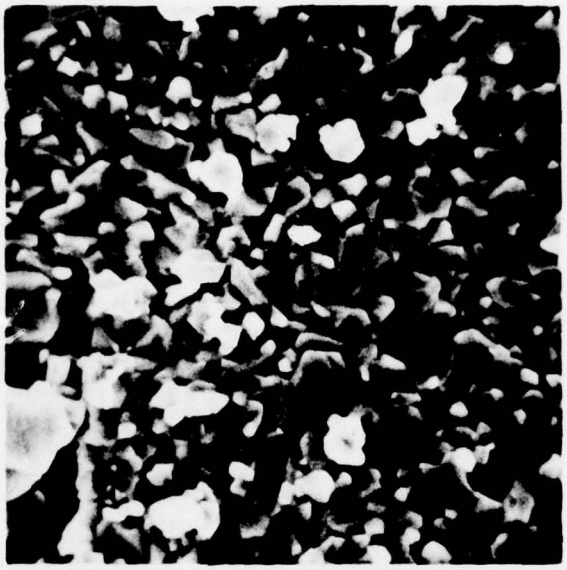


Figure 1. S.E.M. photograph.
Batch #102.

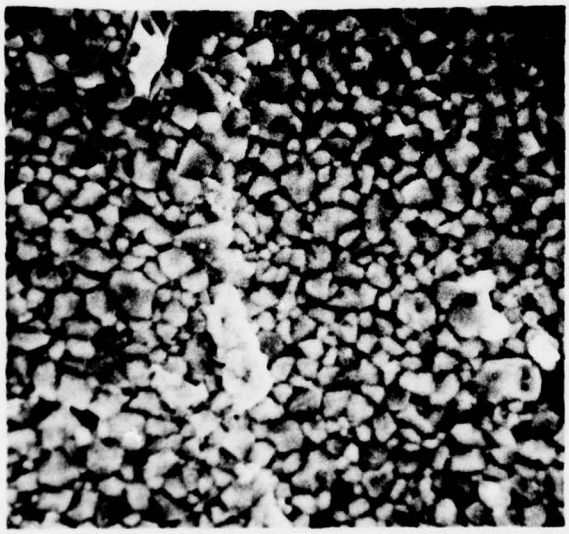


Figure 2. S.E.M. photograph.
Batch #104.

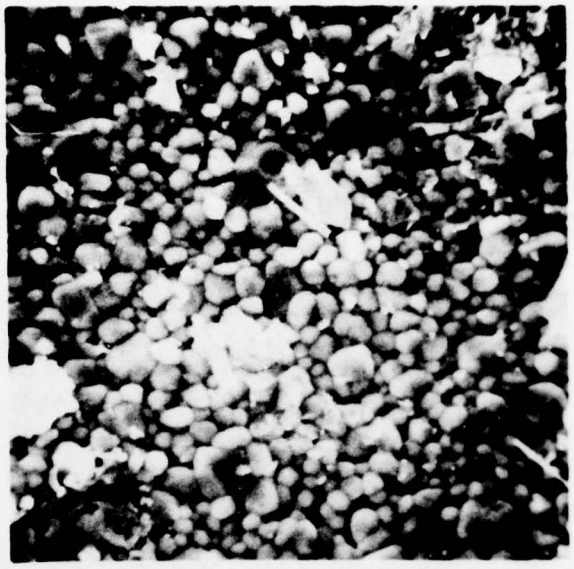


Figure 3. S.E.M. photograph.
Batch #105.

A S.E.M. picture of the cleaved cross-section of a NbO chip, Batch #105 is shown in Figure 4. The magnification is 20X and the rectangular piece in the center of the picture is actually 4.0 mm long by 0.7 mm thick. The NbO_2 surface layer can be seen edge-on around the periphery. The fine white lines on the face of the rectangle are the NbO cleavage steps.

Figure 4. Cleaved NbO/NbO_2 chip. Batch #105.

In Figure 5 the edge-on view of the NbO_2 layer at 2000X magnification for Batch #105 is seen. The picture was taken at a tilt angle of about 10° with respect to the (010) cleavage plane of the chip. The measured NbO_2 layer thickness is 11 to 12 microns.

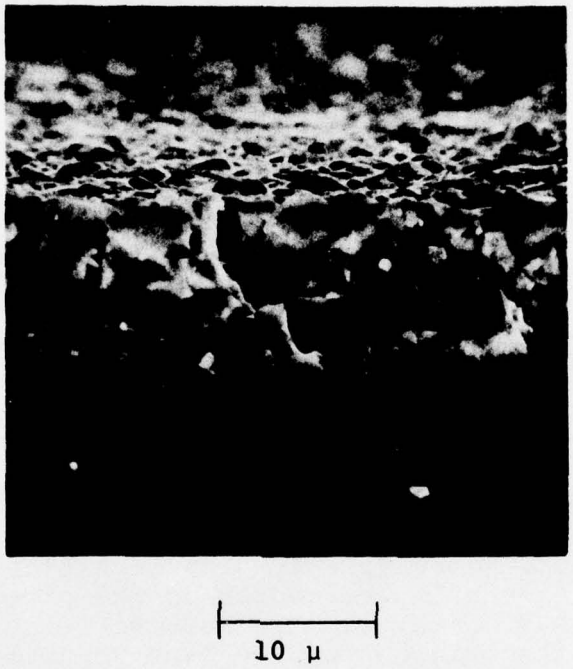


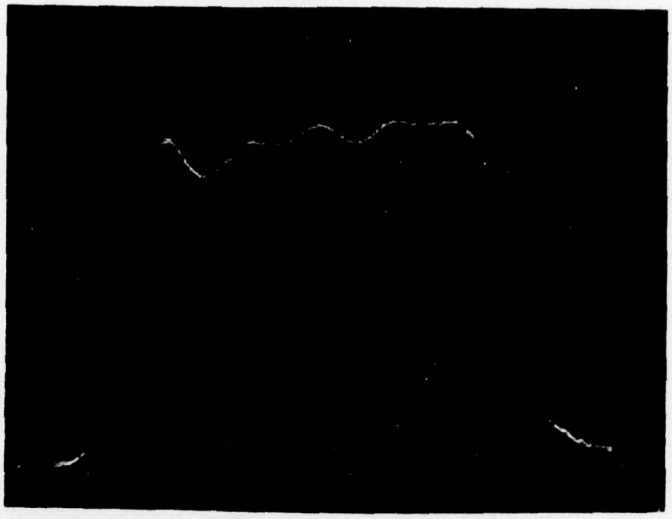
Figure 5. NbO_2 layer edge on.
Batch #105.

Finally, it should be noted that the chips as supplied varied markedly in thickness and diameter. This makes device assembly difficult insofar as package size must be compatible with a highly variable chip size. Cleaved chips are probably unsuitable for a completely mechanized manufacturing process.

III. TEST SETUP

A fast rise time system to test the switching characteristics of the NbO/NbO_2 devices was assembled. The system comprises a #503A SKL cable pulser with pulse rise time of about 400 ps. Maximum rated pulse height is 500 V and pulse width can be varied from 3 to 100 ns. Pulse repetition rates of up to 125 Hz can be achieved. The pulse is fed into a GR-874 system and after appropriate attenuation (usually a factor of 1000) the signal is measured using a sampling scope. Currently, a Tektronix 564B storage scope with type 3S2 sampling unit is being used. Effective rise time for the detector is 75 ps.

The system response is shown in Figure 6 for a 3 ns pulse. The pulser cable was charged to 1000 V and a reasonably square pulse (risetime 400 ps, amplitude 500 V) was obtained.



100 V/div

500 ps/div

Figure 6. System response for 3 ns pulse.

The system was calibrated using a coaxial microwave resistor in parallel with the pulser. Figure 7 gives the wave form with a parallel resistance of 5 ohm and the pulser cable charged to 1000 V as before. The pulse shape is well preserved indicating (as expected) no inductive effects for a coaxial shunt resistance. The pulse amplitude is now 80 V, implying a current I of 80/5 = 16 A through the shunt resistance. This value compares well with the calculated value of

$$I = (V_{cable} - 2V_{device})/50$$

$$= (1000 - 160)/50$$

$$= 16.8 \text{ A}$$

The system has been calibrated using a set of such shunt resistors.

To measure insertion loss of the device in the off state a Hewlett Packard type 431B power meter fed by an appropriately attenuated Hewlett Packard type 608E VHF signal generator is currently being used. This system has a resolution of better then 0.05 dB up to 480 MHz.

IV. PACKAGING CONFIGURATIONS

Even assuming an ideal device (i.e., a perfect short in the on state) it is clear that inductive effects can cause a voltage spike to occur for a coaxial cable with a non-coaxial short. Consider for example the configuration of Figure 8. Here the coaxial cable is shorted with a foil strip, length 1.4 inch and width 1/8 inch. The result obtained when pulsed with a 3 ns 250 V pulse (cable charged to 500 V) is given in Figure 9. The observed

20 V/cm

500 ps/div

Figure 7. Voltage across 5 Ω coaxial microwave resistor. Applied pulse 500 V, 3 ns.

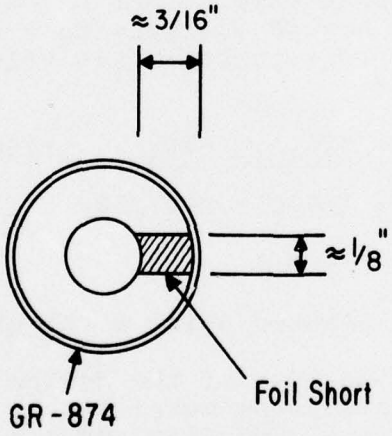


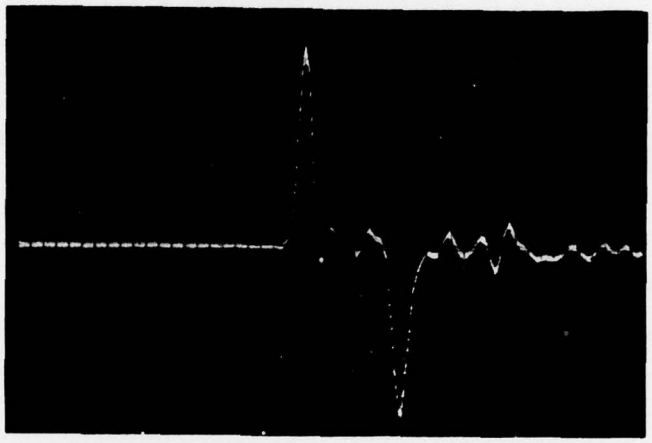
Figure 8. Foil strip short between center and outer conductor of GR-874 line.

voltage spike (30 V) is not surprising if the inductance L of the foil short is calculated.[7] It is found that $L = 1.6 \times 10^{-9}$ and hence expected that a voltage spike of

$$L \frac{dI}{df} \simeq L \frac{V_{cable/50}}{\text{pulse rise time}} = 1.6 \times 10^{-9} \frac{500/50}{0.4 \times 10^{-9}} = 40 \text{ V},$$

7. F.E. Terman, Radio Engineers Handbook, McGraw Hill New York (1943).

in good agreement with observation. Of course the magnitude of the inductive spike will be proportional to V_{cable}. Thus if V_{cable} = 2000 V (1000 V pulse) an inductive spike of 160 V is expected. Also noted are the presence of ringing oscillations (~ 4 V, Figure 9). These oscillations do not occur in a properly coaxial system.



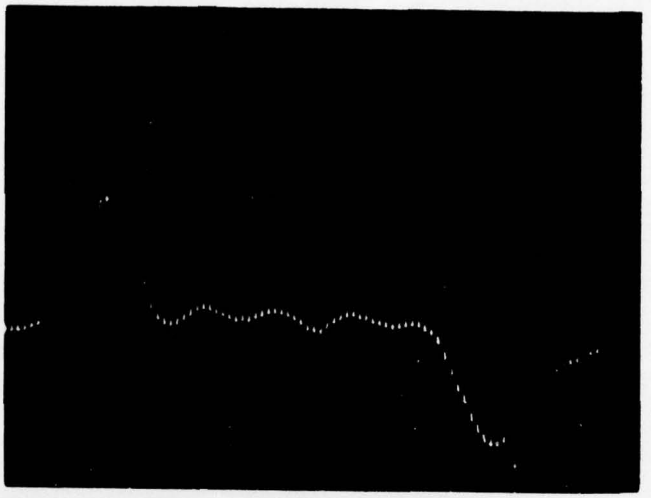
10 V/div

2 ns/div

Figure 9. Inductive spike from the foil shorting strip of Figure 8. Applied pulse is 250 V, 3 ns.

In Figure 10 is given the inductive spike resulting when a shorted 1N23 type diode package is used. In this case the tungsten catswhisker was allowed to contact the package base. The diode package base was inserted into a hole drilled in the center GR874 line and a pulse of 500 V, 3 ns applied. The resultant inductive spike is 200 V and it is thus clear that all attempts to protect microwave receivers with this package at a less than 200 V level are futile (unless the system bandwidth is too low to accept such an inductive spike).

It is apparent from the above discussion that it is difficult to avoid significant inductive spikes using a single sided shunt between center line and ground in a coaxial system, subjected to fast rise time, high voltage transients. Sophisticated solutions can be envisaged to this problem. However, it was chosen to proceed temporarily with a single sided shunt configuration for the preliminary diode package since it is the initial goal



100 V/div

500 ps/div

Figure 10. Inductive spike from shorted 1N23 package (catswhisker type). Applied pulse is 500 V,3 ns.

to characterize the behavior of the NbO/NbO_2 switching material. Where necessary, any background inductive spikes can be subtracted out to display the intrinsic material behavior. The detailed packaging system used will be given below.

V. POINT CONTACT CONFIGURATION

In order to gain an idea of the compatibility of the measurement system described in Section III with previous work, the response of NbO/NbO_2 chips mounted in 1N23 type diode packages was briefly investigated. In this case, pressure contact was made to the NbO_2 surface with a tungsten catswhisker.

Contact of the NbO/NbO_2 chip to the package base was made using the following procedure. The reverse side of the NbO/NbO_2 chip was lapped with a SiC grit/water slurry to expose the conductive NbO. The sample was cleaned in acetone and methanol and dried and bonded with electrically conductive epoxy to the package base stud. The epoxy was cured at 150 °C for 10 minutes.

Figure 11 gives a typical result for a NbO/NbO_2 chip mounted using tungsten pressure contact when subject to a 500 V,3 ns pulse (cable charged to 1000 V). The packaged device switches, reaching its maximum voltage $V_{th} \tilde{} 500$ V about 500 ps after the onset of the pulse.* About 200 V of this V_{th} should be attributed to the inductive spike resulting from this kind of sample packaging (see Figure 10). Also noted was the evident jitter in the trace. This jitter was usually (though not invariably) present in point contact samples.

*For a definition of threshold switching voltage, as used in this report, see Section XIV.

100 V/div

500 ps/div

Figure 11. Switching of point contact configuration for NbO/NbO_2 device. Applied pulse 500 V, 3 ns. Sample L-7.

In Table 1 D.C. resistance and insertion loss as a function of the number of pulses are given. Little insertion loss is evident. The variations observed in the value of the sample attenuation is probably due to experimental drift in the power meter.

TABLE 1. PULSE BEHAVIOR OF SAMPLE L-7 (point contact configuration) Sample was subjected to repeated pulsing at the 3 ns, 500 V level.

# of Pulses	D.C. Resistance kΩ	480 MHz Insertion Loss (dB)	200 MHz Insertion Loss (dB)
0	204	0.06	0.05
10^3	113	0.03	0.04
3×10^3	22	0.09	0.1
5×10^3	7.1	0.06	0.04

Figure 12 gives similar measurements upon a different (L-6) point contact sample. In this case V_{th} (including the package) is 380 V. This case and the baseline curve of Figure 10 has been digitized to evaluate the sample response alone and this is plotted in Figure 13. As expected, for this sample the threshold voltage (excluding the point contact package) is approximately 200 V.

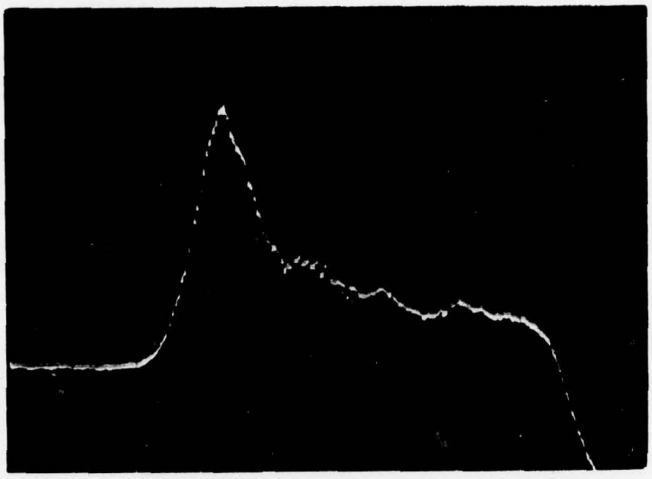


Figure 12. Switch of point contact configuration for Sample L-6. Applied pulse. 500 V, 3 ns.

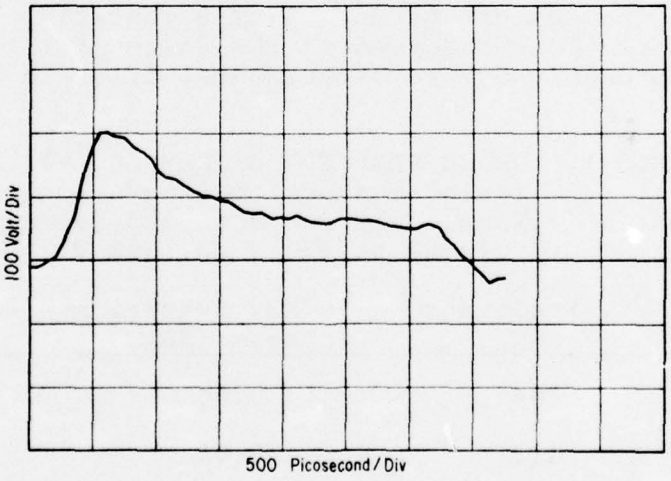


Figure 13. Data of Figure 12, digitized and corrected for package inductance.

In Table 2 ,the resistance and insertion loss data for sample L-6 are given. Note that the insertion loss has increased quite substantially after 3000 pulses. Figure 12 was obtained after 3000 pulses.

Table 2. PULSE BEHAVIOR OF SAMPLE L-6
(point contact configuration)
The sample was subjected to
500 V, 3 ns pulses.

# of Pulses	D.C. Resistance kΩ	480 MHz Insertion Loss (dB)	200 MHz Insertion Loss (dB)
1.5×10^3	3.7	0.06	0.07
3×10^3	0.5	0.6	0.3
4.5×10^3	0.4	0.5	0.5

The insertion loss α may be computed from $\alpha = -20 \log_{10} [2R/(1+2R)]$ where $R = Z/Z_o$. Since it appears that any capacitative shunting of the packaged device may be neglected (see e.g., Table 1), for an off state resistance of 0.5 KΩ, α = 0.4 dB. This agrees well with the data of Table 2.

Also, it might be noted at this point that while quite erratic and variable values were obtained for the sample D.C. resistance and degradation with pulsing, almost all devices examined exhibited threshold voltages in the 400-500 V range (including package effects). Subtracting out the inductive spike due to the catswhisker package would then imply that the threshold voltage for the *NbO/NbO_2 device itself was in the* 100-300 V range.

Finally, it is noted that an examination of the contact area between the NbO_2 layer and the tungsten whisker for pulsed samples was made. A distinctly eroded spot, about 0.001" in diameter was typical of the contact interface. It is therefore clear that the current (whether filamentary or not) during the switching process was restricted to an area of less than $10^{-5}cm^2$. The temperature rise ΔT, in such an area when pulsed may be computed. A pulse of 3 ns width and 200 V amplitude across the switched device was assumed. As a good approximation the device current ≃ 12 A. The high temperature volume specific heat of NbO_2 is about 3.5 J cm^{-3} $°C^{-1}$ and the x-ray density ρ = 5.916 gm/cm^2. Using these values, it is found that:

(1) Energy input to sample per pulse = 7×10^{-6} J. Volume of sample conducting current < 5×10^{-9} cm^3.

$$\Delta T > \frac{3 \times 10^{-5}}{3.6 \times 5 \times 10^{-9}} \quad °C \simeq 400 \ °C$$

Since switching to the metallic state occurs at 800 °C in NbO_2 it is tempting to conclude that the switching observed is in fact thermal. Filament widths of < 0.001" are common in amorphous switching devices, and if this were the case here the

NbO_2 would clearly reach its metal-semiconductor transition temperature.

VI. PACKAGING

To avoid the problems inherent in a point contact packaging configuration an attempt was made to mount devices using evaporated Al contacts. The device preparation procedure is as follows:

One side of the NbO/NbO_2 chip is lapped, cleaned and dried as described in Section V to expose the NbO layer. An array of 0.005" diam. Al dots is evaporated on the NbO_2 surface. The Al layer is 1/2-1μ thick. The exposed NbO face of the chip is then epoxied to a microwave diode package of the type illustrated in Figure 14.

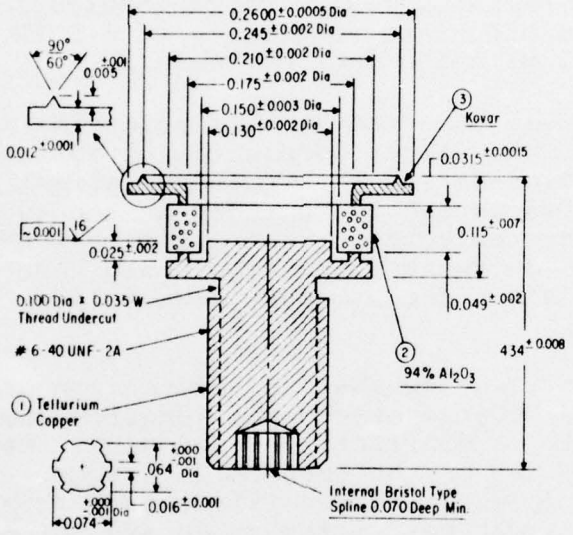


Figure 14. Microwave diode package used for mounting NbO/NbO_2 chip. Various dimensions are available.

A connection between the 0.005" Al electrode and the rim of the diode package is made by means of an 0.001" fine gold wire. The wire is balled at one end (ball size 0.002-0.003") and cold-welded to the Al dot using pressure and ultrasonic energy.

The completed device is screwed into the holder shown in Figure 15 for pulsing and power loss measurements. The holder is compatible with GR-874 components and adapters are available to convert the GR-874 "tee" to type N.R.F. fittings.

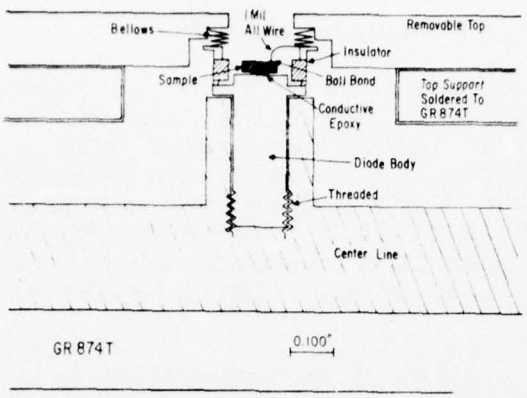
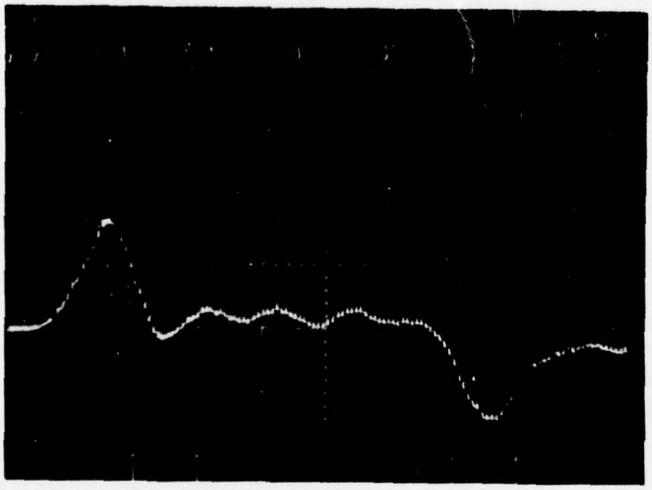


Figure 15. NbO/NbO_2 chip mounted in diode package which fits into specially adapted GR-874 "tee".

Figure 16 gives the voltage versus time of such a package with no NbO/NbO_2 chip i.e., the gold wire is bonded directly to the microwave diode package base. An inductive spike of about 160 V is observed. This is somewhat better than the 1N23 cats-whisker type configuration, but as has been emphasized, any single sided short will produce a non-negligible inductive spike for sufficiently fast rise time pulses. It was chosen to use the package of Figures 14 and 15 and subtract out the package effect where necessary in investigating the NbO/NbO_2 devices.



100 V/div

500 ps/div

Figure 16. Inductive spike from the shorted diode package of Figure 15. Applied pulse 500 V, 3 ns.

VII. NbO/NbO_2 DEVICES WITH Al CONTACTS

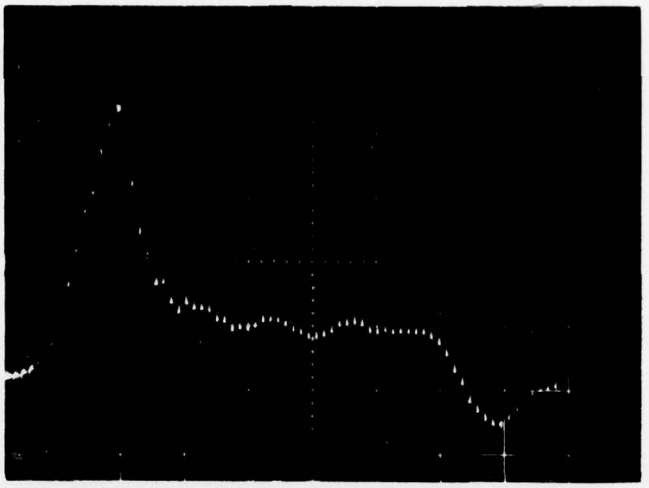
The results obtained with the Al contacted NbO/NbO_2 devices are quite variable. One measure of the variability is the D.C. resistance R between the as-evaporated dots on the chip face and the NbO base contact. This resistance R has been probed for a chip mounted on the diode package but not yet wire bonded. Some results are given in Table 3. It is noted that the value of R is highly variable, both from sample to sample on the same batch (Yeshiva Lot #110) and even variable on the face of a single sample (X-3-7).

TABLE 3. VALUE OF D. C. RESISTANCE R AT VARIOUS POINTS ON THE CHIP FACE FOR THREE NOMINALLY IDENTICAL SAMPLES. An array of 0.005" diameter Al dots was evaporated on the sample face.

Dot #	Sample X-3-6 R (kΩ)	Sample X-3-7 R (kΩ)	Sample X-3-3 R (kΩ)
1	217	15	0.31
2	350	1.2	0.51
3	85	0.45	0.52
4	115	0.47	0.60
5	104	3.4	0.74
6	113	8.4	1.0
7	156	279.0	-
8	215	641.0	-
9	135	3.0	-
10	210	1.2	-

Figure 17 gives the switching curve obtained on a sample (X-3-4B) with Al contacts. Threshold voltage was 450 V and no jitter was observed. Figure 18 gives the data with the package inductance (Figure 16) subtracted out. The true device threshold voltage is about 300 V and an "inductive" type initial peak characteristic of NbO/NbO_2 switching persists. Figures 19 and 20 give the switching behavior (sample X-2-3) with and without the package inductance, respectively. In this case the device threshold is lower (~ 150 V). The spike in Figure 19 is largely a package effect.

Figure 21 gives the voltage time trace for sample X-3-4 subjected to a 3 ns, 500 V (cable = 1000 V) pulse. This photograph was taken after 500 pulses had passed the sample. Figure 22 gives the characteristic for this sample with the package inductance subtracted. It is interesting to follow the degradation of this sample with pulsing. In Table 4 is given the resistance and insertion loss at 480 MHz for various types of pulsing.



100 V/div

500 ps/div

Figure 17. Switching in sample X-3-4B. Applied pulse 500 V, 3 ns.

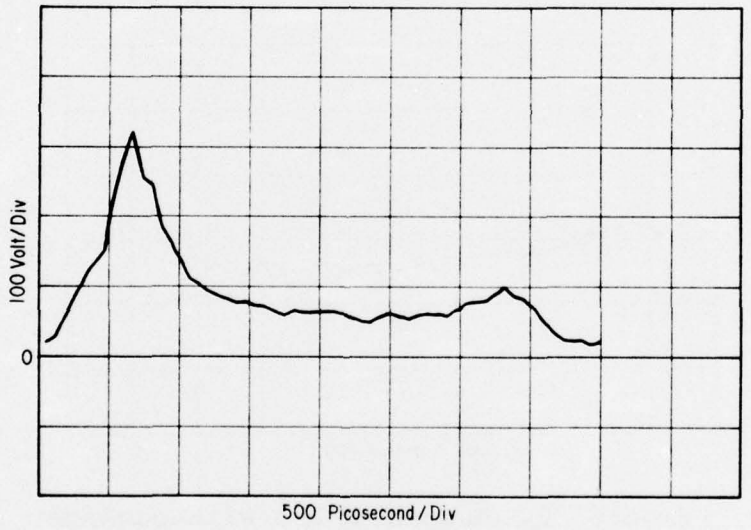
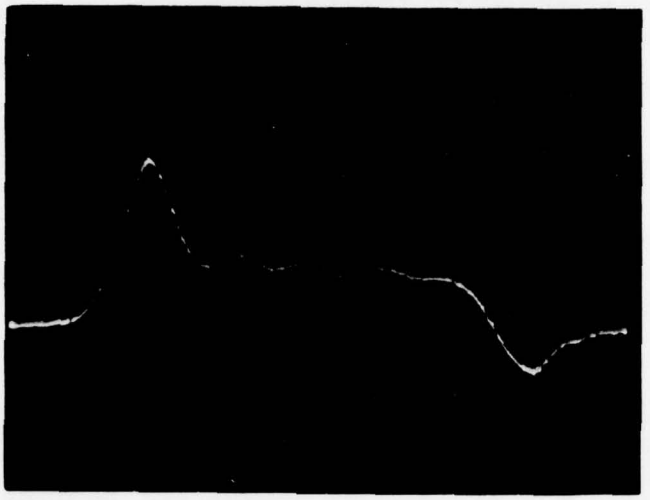


Figure 18. Sample X-3-4B with package inductance removed.



100 V/div

500 ps/div

Figure 19. Sample X-2-3. Applied pulse. 500 V, 3 ns.

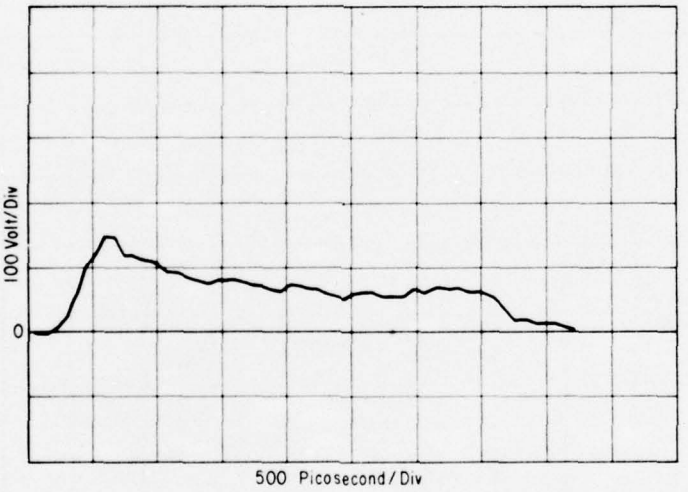
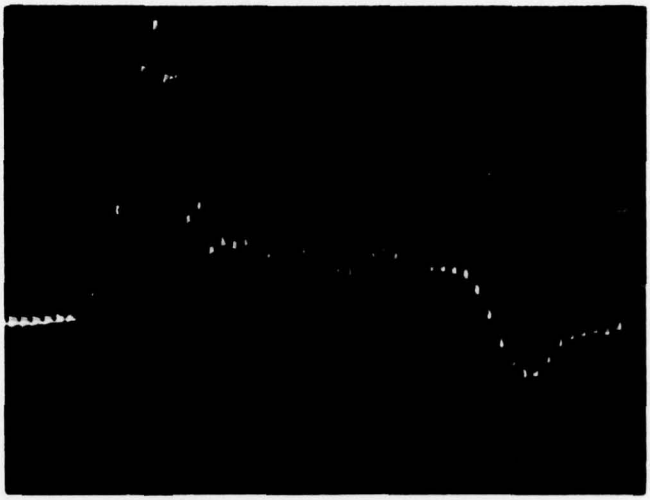


Figure 20. Sample X-2-3 with package inductance removed.

100 V/div



500 ps/div

Figure 21. Sample X-3-4. Applied pulse 500 V, 3 ns.

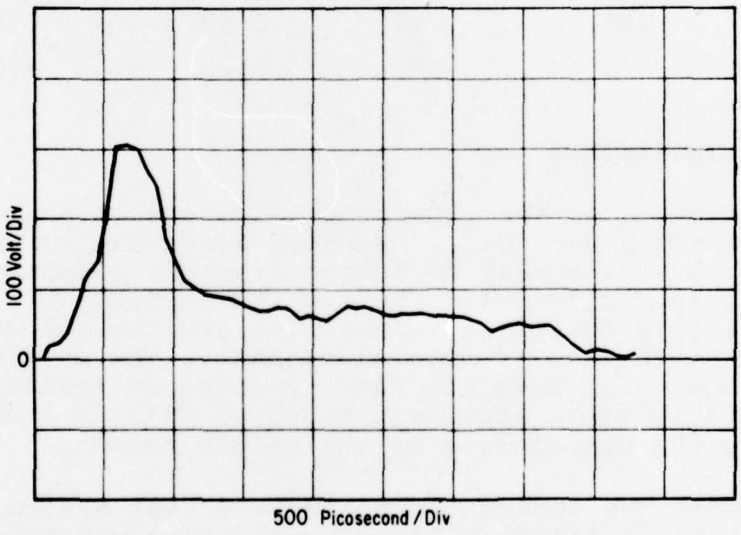


Figure 22. Sample X-3-4 with package inductance removed.

From the data it is clear that the sample undergoes substantially accelerated degradation when the pulse width is increased. This behavior is typical for samples with evaporated Al contacts.

TABLE 4. BEHAVIOR OF SAMPLE X-3-4 WITH REPEATED PULSING

# of Pulses	Pulse Height (V)	Pulse Width (ns)	D.C. Resistance (kΩ)	480 MHz Insertion Loss (dB)	Comments
0			208	0.1	
250	500	3	1.07	0.09	
250	500	3	95	0.09	
250	250	3	-	-	No Switching
250	250	3	97	0.09	No Switching
250	375	3	-	-	Partial Switching
250	375	3	-	-	Partial Switching
250	500	3	58	0.09	
250	500	10	2.8	0.18	
250	500	10	0.83	0.36	
500	500	50	0.007	8.0	Sample Failed

VIII. EFFECT OF TEMPERATURE

An evaluation of the effect of temperature upon switching of NbO_2/NbO chips has been made. Samples were mounted with silver epoxy and gold wire bonded to 0.005" diameter evaporated Al dots as described in Section VI. The mounted samples were fixed in the holder previously described (Figure 15) and the holder in turn was placed in a Statham environmental chamber. The environmental chamber was cooled using cold CO_2 gas. Heating is resistive in an air ambient. Sample temperature was measured using a thermocouple connected to the ground line of the sample holder.

The sample was connected to the 50 Ω test system using moderately long (3 ft) flexible cables. Care was taken to ensure that the pulse waveform was not degraded in this setup. Power measurements using this configuration and a power meter were found to be untrustworthy, presumably due to imperfect contacts and cable losses. Therefore, it was chosen to characterize the NbO_2/NbO 500 MHz insertion loss using D.C. resistance measurements. There is excellent correlation between the D.C. and 500 MHz measurement techniques as indicated in Tables 1 and 2.

In Table 5 a typical measurement sequence is given. The pulse applied was 500 V amplitude, 3 ns duration at 50 Hz repetition rate. The virgin sample was measured and found to have resistance 35.8 KΩ at room temperature. This may be compared with a computed value of 48 KΩ, using the literature[8] room temperature resistivity value of 6.3 KΩ parallel to the C axis. Two hundred-fifty (250) pulses reduce R to 1.14 KΩ (Figure 23). (Note that α = 0.4 dB corresponds to a shunt resistance of 0.53 KΩ, ignoring capacitive effects.) Raising the temperature to 83 °C then drops R to 0.78 KΩ

TABLE 5. EFFECT OF TEMPERATURE UPON NbO_2/NbO Switching

Experiment Sequence	No. of Pulses Applied	D.C. Resistance (KΩ)	Temp. °C	Fig. No.
1	Initial	35.8	26	
2	250	1.14	26	23
3	None	0.78	83	
4	250	0.42	83	24
5	None	1.43	-54	
6	250	0.85	-54	25
7	None	.733	26	
8	250	1.1	26	26

Figure 23. NbO_2/NbO chip No. X-3-9 Temperature = 26 °C.

(8) G. Belanger, J. Destry, G. Perluzzo and P.M. Raccah, Canad. J. Phys. 52, 2272 (1974).

Figure 24 gives the result of pulsing the device at 83 °C. The switching characteristic is basically the same as that of Figure 23, indicating little or no temperature dependence of the switching characteristic.

Further pulsing degrades the sample resistance to 0.42 KΩ. Cooling to -54 °C increases R to 1.43 KΩ and Figure 25 confirms the basic insensitivity of the switching curve to temperature. Figure 26 gives the switching characteristic upon returning to room temperature.

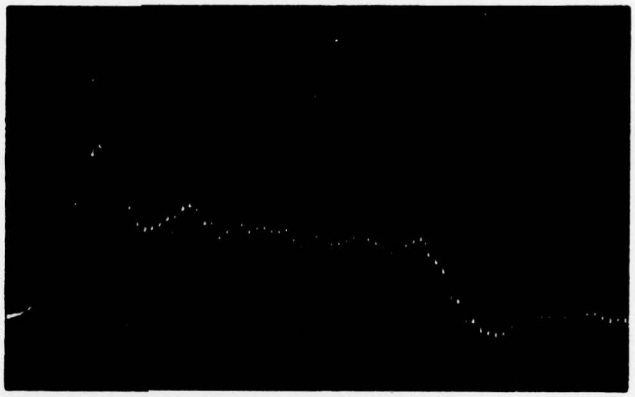


Figure 24. NbO_2/NbO chip No. X-3-9 Temperature = 83 °C.

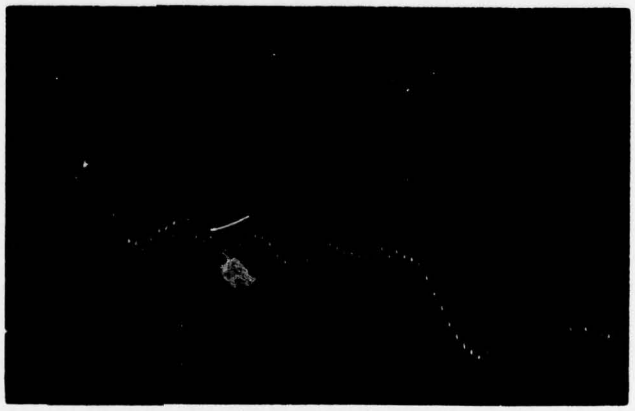


Figure 25. NbO_2/NbO chip No. X-3-9 Temperature = -54 °C.

Figure 26. NbO_2/NbO chip No. X-3-9 Temperature = 26 °C.

From Table 5 it is concluded that the resistance of a "switched" sample varies only a factor of 3 between +83 and -54 °C.[18] This is surprising in view of the 0.48 eV activation energy[18] for the low field resistivity of NbO_2 which implies a resistance variation of about a factor of 10^4 in this temperature range. It is presumed that the switched sample is degraded in a way which makes the conducting region more "metallic". Confirmation of this general picture is made by noting that NbO_2/NbO samples with a higher resistance (whether switched or not) generally exhibit a much greater drop in resistance with increasing temperature.

IX. CONTACT PROCEDURES

It is feasible that the rapid deterioration with pulsing (and especially so for pulses ~ 50 ns long) of the NbO/NbO_2 chips is a result of an electrode-NbO_2 reaction. To date, evaporated Al electrodes approximately 0.5 μ thick have been used as contact electrodes. An "ideal" electrode system might use Nb metal as the electrode material. Nb is refractory and very difficult to evaporate. Therefore, a sputtering technique was utilized to provide 0.005 inch diameter contact electrodes to the NbO/NbO_2 chip. The detailed experimental procedure is described below:

1) The as received chips are examined under a microscope and those with at least one relatively flat surface selected. Ridges left on the chips during cleaving, preclude good sample to mask contact necessary in the electrode deposition process.

2) The samples are mounted flat side down on a glass plate fastened to a lapping jig. The samples are held securely to the glass by glycole phthalate ($C_{12}H_{12}O_5$-a low melting point (~100 °C) polyester). Mounting is performed with the jig and samples on a hot plate, T ~ 150 °C.

3) Small glass bars are also secured to the glass plate (using glycole phthalate) which effectively surround the samples as shown in Figure 27. The glass bars (of known thickness) are important in the grinding and polishing step below. They help keep the sample surface flat and are used to estimate the lapped sample thickness.

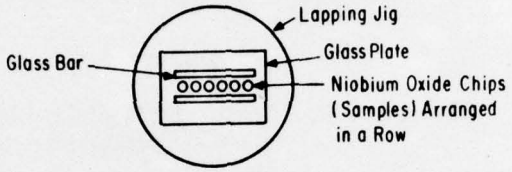


Figure 27. Schematic drawing of sample holder used in grinding and polishing step.

4) The samples are ground with 280 mesh carborundum grit and polished with 5 μ particle size carborundum powder. In this step, all the NbO_2 is removed from the lapped side. The samples are flat and of uniform thickness ~ 15-25 mils.

5) The samples are removed from the lapping jig by heating. They are then rinsed 3 or more times in hot acetone with ultrasonic agitation. This removes all traces of glycole phthalate from the samples.

6) The samples are rinsed in hot methyl alcohol and blown dry in nitrogen.

7) The samples are placed lapped side down on a glass plate in the sputtering apparatus as shown in Figure 28. Each sample is separately covered with a thin molybdenum mask having 5 mil diameter holes on 20 mil centers. (The small masks were made by dicing a large 1" x 1" mask.) Since the mask must essentially contact the sample it is important that the cleaved surface be free of ridges. A pure niobium sputtering target is attached to the high voltage fixture.

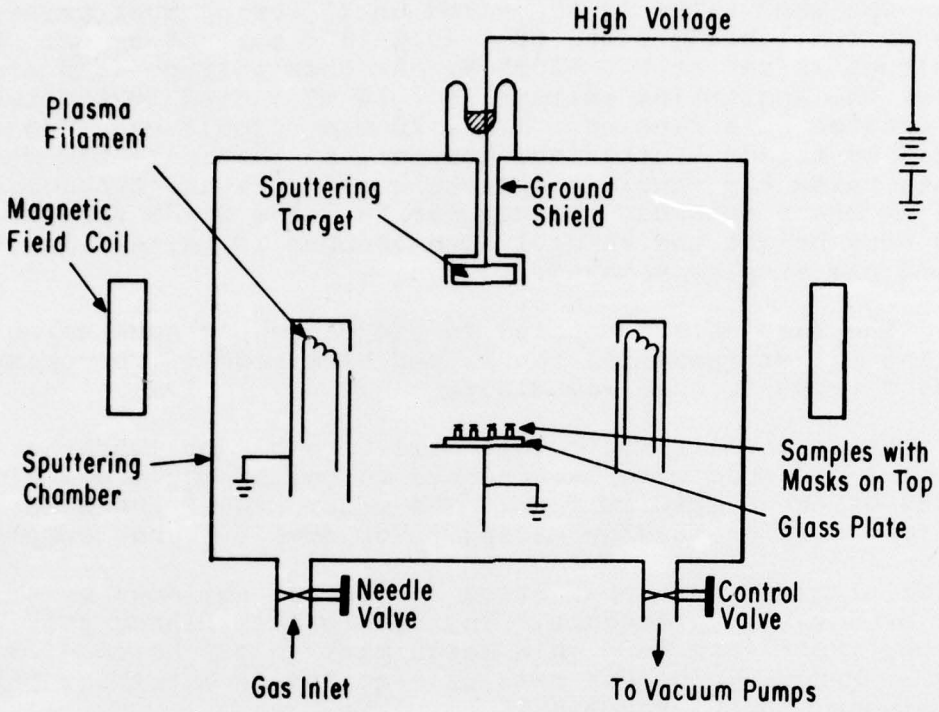


Figure 28. Schematic drawing of sputtering apparatus.

8) The sputtering chamber is pumped out using a mercury diffusion pump (no oil contamination). The chamber is crudely outgassed by operating the plasma filaments (which heats the chamber). When the chamber attains a vacuum of ~ 10^{-6} torr the sputtering process can be started.

9) Argon gas is introduced into the sputtering chamber through a needle valve. The flow is adjusted so that the chamber pressure with the valve to the pumps fully open, is ~ 3 x 10^{-3} torr.

10) Using the D.C. triode technique, niobium metal is sputtered into the samples through the 5 mil holes in the mask. The sputtering voltage is set at -2000 V and the plasma filament current adjusted to give a sputtering current of 20 mA. (Low voltage plasma ~ 30 V and ~ 1 A) Niobium is sputtered for 30 minutes at a rate of ~ 7000 Å/30 min.

11) After niobium deposition, the pump valve is closed and the chamber back-filled with argon to 1 atmosphere pressure. The chamber is opened and the niobium sputtering target replaced with a gold target. The system is again pumped down and steps 8 and 9 above are repeated. (Care must be taken to make sure samples and masks are not disturbed.)

12) The pump valve is throttled until the chamber pressure reaches an equilibrium value of ~ 40 x 10^{-3} torr of argon. The high voltage is set at V ~ -2000 V. At this voltage (and argon pressure) the sputtering current is ~ 14 mA. Gold is sputtered for 10 minutes at a rate of ~ 1.2 μ/10 min. (Gold can also be deposited by triode sputtering; however, in this case the plasma filaments raise the sample temperature slightly and the deposited gold layer has a tendency to agglomerate. The diode sputtered gold is very bright and shiny.) The chamber is back-filled with argon and the samples removed.

13) The samples are mounted in the diode packages using conducting silver epoxy (on the lapped back side). The epoxy is cured at T ~ 180 °C for ~ 10 minutes.

14) Using an ultrasonic gold ball wire bonder (Mech-El, NU823), a 1 mil gold wire is attached to one of the 5 mil niobium-gold dots on the sample surface. The other end of the wire is bonded to the diode package casing. The device is now complete.

(For aluminum contacts, steps 7 - 12 are replaces by a much simpler evaporation procedure. The samples are placed above the Al source, front face down on a large mask (5 mil holes - 20 mil centers). Hence, much less care is required in obtaining back side flatness and thickness uniformity.)

Using the above procedure a group of NbO/NbO_2 chips were electroded (all Batch #102) with sputtered Nb/Au contacts. In addition, a control group of samples from Batch # 102 was electroded with evaporated Al contacts.

Table 6 below gives the results of pulsing a sample with Nb/Au contacts. After 500 pulses of 3 ns duration the resistance decreases from 15.4 to 0.97 KΩ. Further pulsing with a longer pulse width apparently increases the sample resistance. It is presumed that either part of the electrode has been burned off or that a new filament is now operating in the NbO_2 layer. Figure 29 gives the initial switching characteristic of this sample. It may be noted that there is a great variability among samples regarding the pulse deterioration of the NbO_2/NbO chips. For instance, a sample nominally identical to that of Table 6 with Nb/Au contacts had virgin D.C. resistance 14.1 KΩ, and resistance equal to 1.36 KΩ after 500 pulses of 500 V amplitude, 3 ns duration. However, after 500 pulses of 50 ns duration the sample had shorted (resistance = 2.6 Ω).

TABLE 6. BEHAVIOR OF NbO_2/NbO CHIP WITH Nb/Au CONTACTS

No. of Pulses	D.C. Resistance (KΩ)	480 MHz Insertion Loss (dB)	Pulse Type
virgin	15.4	0.17	
250	8.8	0.23	500 V, 3 ns
350	0.97	0.4	500 V, 3 ns
500	10.0	0.22	500 V, 50 ns
500	6.8	0.28	500 V, 50 ns

Figure 29. NbO_2/NbO chip with Nb-Au contact. Sample No. X-13-4, Batch #102.

In Table 7 the behavior of a sample from Batch #102 with evaporated Al contacts is given. This sample shows basically the same behavior with pulsing as does the sample of Table 6. In Figure 30 is given the initial switching characteristic of the sample of Table 7. It is also noted that the sample to sample variability in degradation characteristics observed for the Nb/Au contact system persists when samples with evaporated Al contacts are used. It is concluded then that the switching characteristics and sample degradation with pulsing of NbO_2/NbO is not a result of the electrode contact system. This behavior is apparently intrinsic to the NbO_2/NbO chip itself.

X. FAILURE MODES - SAMPLES WITH Al CONTACTS

Since the NbO_2/NbO chip devices show some degradation with repeated pulsing, it seemed worthwhile to attempt to observe any physical effects due to the pulsing. The aluminum contact pad would obscure any observation of the NbO_2 layer beneath and therefore the following procedure to lay bare the relevant area of NbO_2 was adopted:

TABLE 7. BEHAVIOR OF NbO_2/NbO Chip With Al Contacts

No. of Pulses	D.C. Resistance (KΩ)	480 MHz Insertion Loss (dB)	Pulse Type
virgin	33.0	0.14	
250	17.3	0.17	500 V, 3 ns
250	20.5	0.17	500 V, 3 ns
500	10.9	0.23	500 V, 3 ns
500	7.7	0.26	500 V, 3 ns

Figure 30. NbO_2/NbO chip with Al contact. Sample No. X-13-7, Batch #102.

a) The NbO-diode package epoxy bond is mechanically broken to remove the NbO_2/NbO chip from the diode package.

b) Using a sharp knife the ball bond pad is popped off the 0.005" diameter Al contact evaporated on the NbO_2 layer. This procedure did not remove any Al from the NbO_2 layer--i.e., the Al-NbO_2 bond is stronger than the Al-gold ball bond.

c) The NbO_2/NbO chip is etched (5 minutes) in an acid bath (composition: 15 parts HNO_3, 30 parts CH_3COOH, 25 parts H_2O, 380 parts H_3PO_4). This procedure almost completely removes the Al contacts.

A control experiment on bonded but unpulsed devices indicated that the etch did not significantly attack the NbO_2 layer. After about 15 minutes in the bath, bonded but unpulsed devices appeared essentially unblemished in the Al contact area. It may therefore be concluded that the above process is suitable for exposing the NbO_2 layer of pulsed devices.

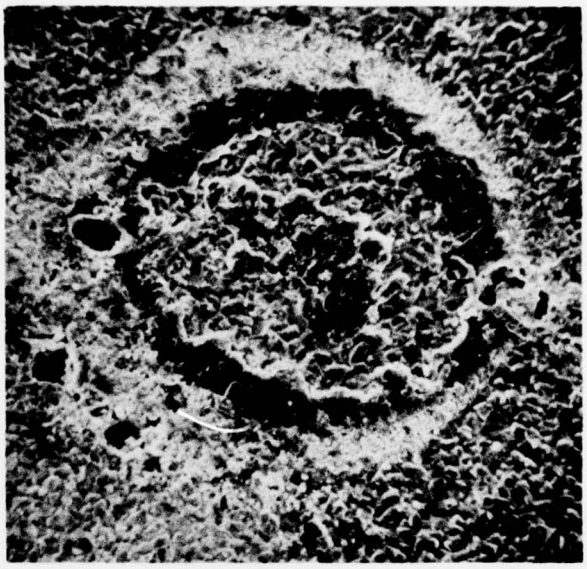
In Figure 31 is given a low magnification shot of the top of an etched NbO_2/NbO chip. Four partially removed Al contact areas are visible. In Table 8 below is listed the pulse history of each area. In Figures 32 - 35 are given high magnification S.E.M. pictures of each of these areas.

50X

Figure 31. S.E.M. photo of NbO_2 layer after removal of gold contact wires and partial etching of the Al contact pads. Four contact areas are visible and regions a,b,c,d are shown at higher magnification in Figures 32,33,34,35, respectively.

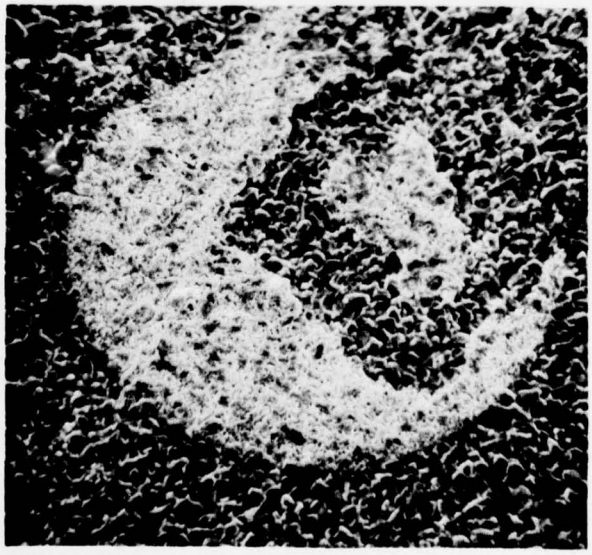
TABLE 8. DAMAGE ANALYSIS - SAMPLE X-14-1

Sample Area	Pulse History	$R_{initial}$ (kΩ)	R_{final} (kΩ)	Observed Damage
a	3000 pulses, 500 V, 3 ns	42	22	4 pits, 5 ~10μ diam. 2-8 μ deep-Fig. 32
b	500 pulses, 500 V, 3 ns	37	0.15	None - Fig. 33
c	1000 pulses, 500 V, 3 ns plus 100 pulses, 200 V, 50 ns	39	0.04	pit, 7 μ deep 10 μ diam. - Fig. 34
d	None - area inadvertently scratched			Fig. 35



500X

Figure 32. S.E.M. photo of contact area "a" of Figure 31. Four pits are visible. Two are on the periphery of the contact area of the gold ball bond, the deeper pit being 6 μ deep and 13 μ in diameter. The two pits close together on the periphery of the Al contact area are 7 μ deep.

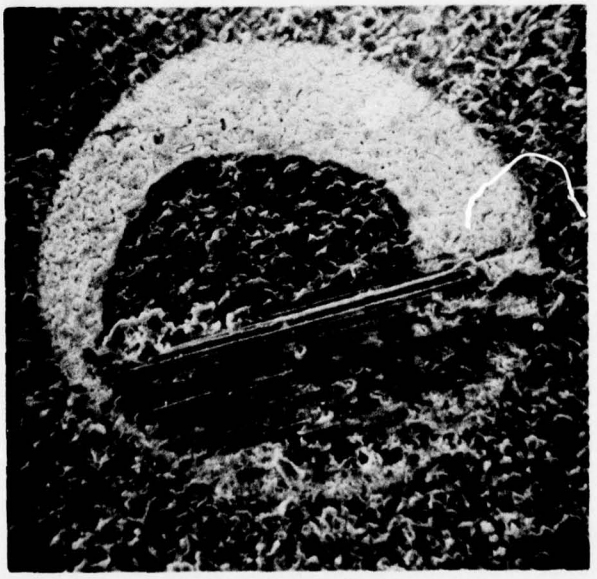


500X

Figure 33. Contact area "b" of Figure 31. No physical damage is visible.

500X

Figure 34. Contact area "c" of Figure 31. Major damage area is pit 10 μ diameter, 7 μ deep, on periphery (between edge of gold ball bond and edge of Al contact) of contact area.



500X

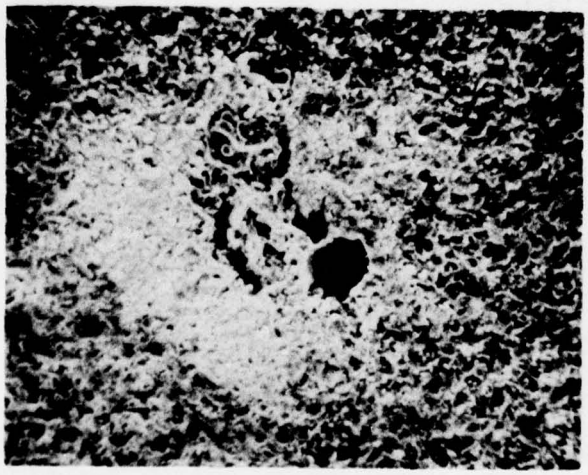
Figure 35. Contact area "d" of Figure 31. This area was inadvertently scratched.

In Table 9 is given the particulars on pulse history and observed damage for other NbO_2/NbO devices. Sample X-6-1 was pulsed using a Velonex Pulse Generator. The massive crater formed presumably results from the energy expanded during the long (10 μs) applied pulse.

TABLE 9. DAMAGE ANALYSIS NbO_2/NbO_2 Chips

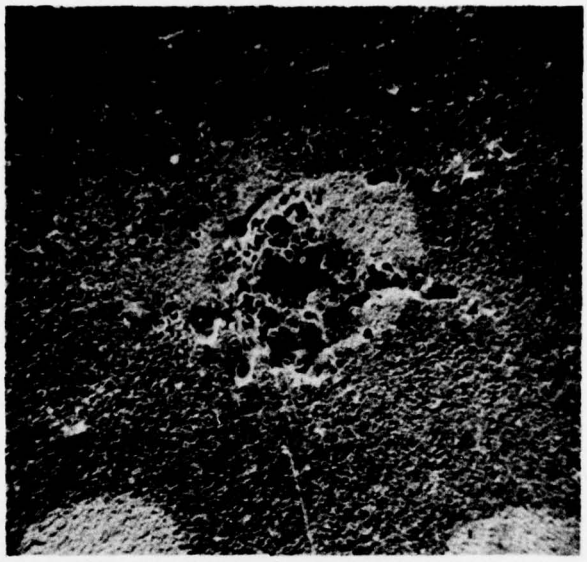
Sample No.	Pulse History	$R_{initial}$ (kΩ)	R_{final} (kΩ)	Observed Damage
X-13-8	750 pulses, 500 V, 3 ns plus 1000 pulses, 500 V, 50 ns	32	1.0	Pit, 13 μ deep, 16 μ diam.-Fig.36
X-6-1	3 pulses, 5 A, 10 μs	10	shorted	Crater-extends beyond contact area-Fig. 37
X-6-1A	750 pulses, 500 V, 3 ns	2.7	0.2	2 pits, 4 μ deep, 8 μ diam.-Fig. 38

From Tables 8 and 9 and Figures 31 - 38 it is concluded that NbO_2/NbO devices with Al evaporated contacts suffer substantial degradation on repeated pulsing. The damage is more severe for 50 ns pulses but some of the devices with numerous 3 ns pulses also exhibit pitting. The multiple pits observed are also consistent with the at times erratic behavior of the off state resistance. Presumably some pits become conducting, short and burn away from the contact, allowing conduction at another location under the electrode.



500X

Figure 36. Sample X-13-8. Major damage is pit 13 μ deep, 16 μ diameter in center of contact area.



200X

Figure 37. Sample X-6-1. This sample was subjected to long duration (10 μs) pulses. The crater formed extends beyond the Al contact area.

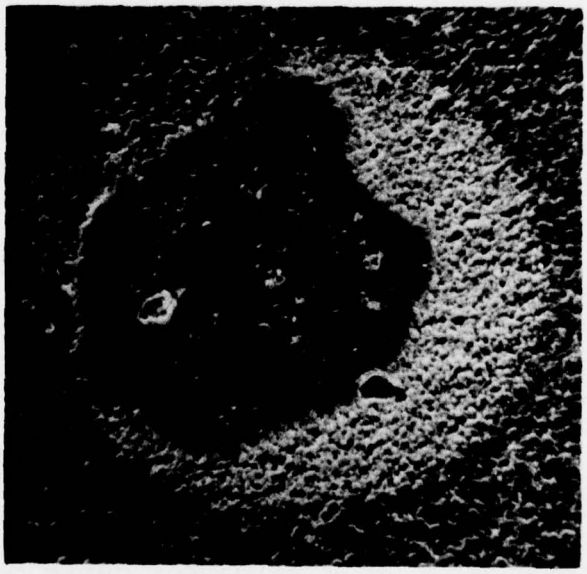


Figure 38. Sample X-6-1A. Two pits, about 4 μ deep and 8 μ diameter are visible.

XI. BACK-TO-BACK DEVICES

To check whether or not the pulse degradation observed in the Al contacted samples was influenced by the contact procedure, "back-to-back devices" were constructed, as illustrated in Figure 39. The devices are made by removing the NbO_2 layer as usual from one side of a NbO_2/NbO chip and inserting two such chips in a 1N23 diode package with their NbO_2 layers touching under light pressure. Ohmic contact is made to the exposed NbO on the back of each chip using conducting epoxy on the NbO crystal.

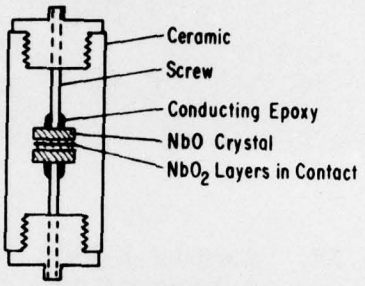


Figure 39. Construction of back-to-back NbO_2/NbO devices.

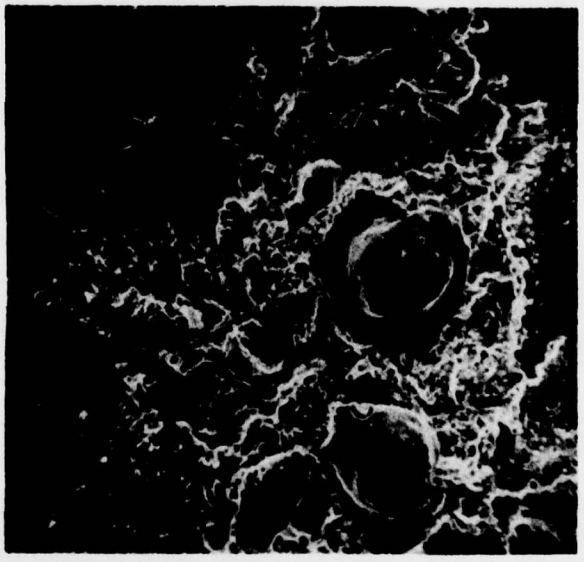
The back-to-back sample would not switch initially under application of a 500 V,3 ns pulse, presumably due to the doubled thickness of the NbO_2 layer. After about 1000 pulses of 50 ns duration, 500 V amplitude, switching of the sample could be induced with 3 ns long pulses. The device was then subjected to about 10,000 pulses of 50 ns duration. This caused the sample off state resistance to drop from its initial value of 10^6 Ω to 1800 Ω. The device of Figure 39 was then disassembled and the NbO_2 surfaces examined for any evidence of pulse damage.

In Figure 40 is given a low magnification S.E.M. photograph of the NbO_2 face of one of the back-to-back chips. Two areas of damage are evident on the chip periphery with the damage region presumably defined by the point of chip to chip contact. In Figures 41a and 41b, higher magnification photographs of area "a" marked in Figure 40 are given. Figure 41a corresponds to the same chip as Figure 40. Figure 41b is the adjacent area of the opposing chip. Note the extensive (matching) cratering of the NbO_2 layer. The major crater of Figures 41a and 41b is about 25 μ deep (i.e., it extends into the NbO crystal) and quite wide, about 40 μ. The extensive damage is expected in view of the quite severe pulse schedule to which the device has been subjected. It may also be concluded that pitting and cratering on the NbO_2 layer in NbO_2/NbO chip devices is inherent to the device, i.e., it is not a function of the chip contact method. Hundreds of 50 ns pulses or thousands of 3 ns pulses cause severe physical damage. Hundreds of 3 ns pulses cause less evident physical

damage but some deterioration in the device off state resistance is at times evident.

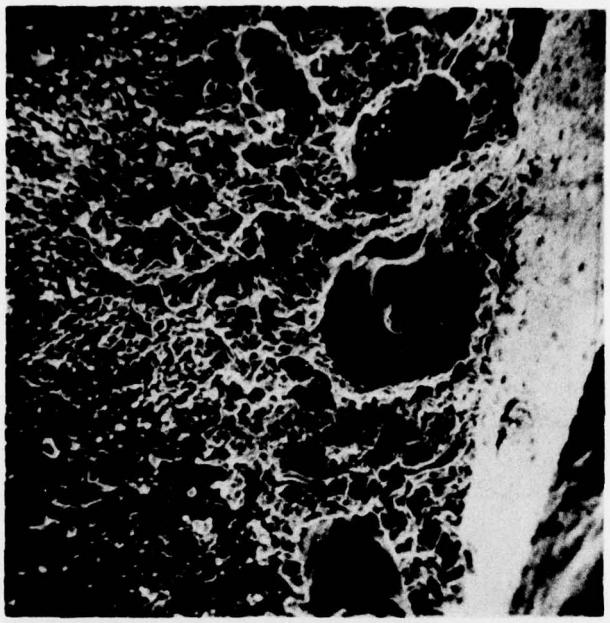
50X

Figure 40. S.E.M. photo of NbO_2 surface of back-to-back device. Two damage areas are indicated.



500X

Figure 41a. Higher magnification photo of damage area a of Figure 40. The major crater is about 25 μ deep.



500X

Figure 41b. Area adjacent to damage region of Figure 41a, but on opposing chip.

XII. FIFTY PRELIMINARY FEASIBILITY MODELS

Fifty mounted coaxial switching devices have been supplied (24 on 10/15/76 and 26 on 12/14/76) which completes item CLIN002.

All devices supplied are derived from Batch #102 of the as received NbO/NbO_2 chips. Device construction which is described in step by step detail in Section IX is summarized below:

1) Remove NbO_2 layer from one side of NbO/NbO_2 chip to expose NbO.

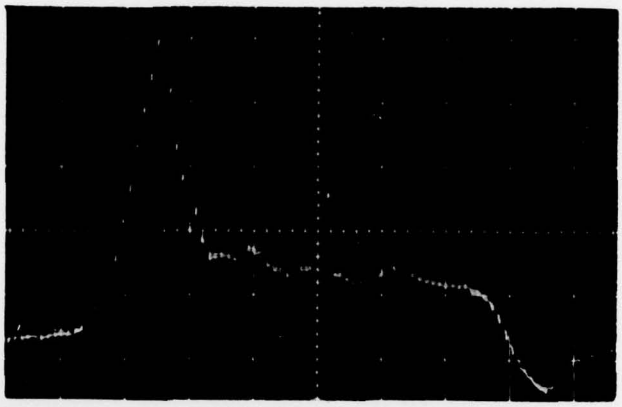
2) Evaporate 0.005 inch diameter Al dot array on NbO_2.

3) Mount exposed NbO surface to microwave diode package with silver epoxy.

4) Bond 0.001" gold wire to one Al dot electrode and connect to diode package lip.

The diode packages and the specially adapted GR874T fitting into which they are inserted for use in 50Ω lines are described in Section VI.

All chips were chosen from Batch #102. D.C. resistance of virgin (unpulsed) samples ranges from 10-70 kΩ. Two randomly chosen samples processed simultaneously with the samples supplied have been characterized electrically. Switching characteristics upon application of a 500 V,3 ns pulse are shown in Figures 42a and 42b.



100 V/div

500 ps/div

Figure 42a. Pulse response of sample X-15-31.

100 V/div

500 ps/div

Figure 42b. Pulse response of sample X-15-32.

In Table 10 data are given for the devices of Figures 42a and 42b. The 500 MHz insertion loss and final D.C. resistance were measured after passage of 250 pulses, amplitude 500 V, duration 3 ns. The device voltage drops to 100-150 V in less than 1 ns after application of the pulse.

TABLE 10. TYPICAL BEHAVIOR OF PRELIMINARY FEASIBILITY MODELS OF COAXIAL SWITCHING DEVICES.

Sample No.	Fig. No.	$R_{initial}$ (kΩ)	R_{final} (kΩ)	500 MHz Insertion Loss (dB)	200 MHz Insertion Loss (dB)
X-15-31	42a	37	16	0.17	0.10
X-15-32	42b	28	4.8	0.20	0.13

XIII. PRELIMINARY STATEMENT OF MANUFACTURING FEASIBILITY

Mounted coaxial switching devices which utilize as received NbO/NbO_2 chips can be made according to the procedures outlined in XII and described in detail in Section VI. A number of "hand" operations are presently required, owing in particular to the differences in physical nature of the as received chips. However, all procedures are straight forward and make use of common, generally available processing and manufacturing equipment and other readily purchasable items such as diode packages. For use in 50Ω GR lines, a specially adapted GR874T "tee" is used into which the diode package is inserted. If large numbers of these are required, special arrangements with the manufacturer of GR fittings to produce such modified units could probably be made.

XIV. THRESHOLD SWITCHING VOLTAGE

Throughout this report has been used the term threshold switching voltage V_{th} to denote the maximum voltage which appears across the device (in response to a voltage pulse) in its low impedance or switched state. This definition follows from Figure 1 of the Technical Guidelines DAAB07-76-Q-1335. For the devices made from ECOM chips and described in this report, the threshold switching voltage is typically 100 to 300 V (when corrected for package inductance) and occurs within the first nanosecond of the applied voltage pulse. However, the voltage necessary to switch the material to its low impedance state may be considerably larger than the threshold switching value. This is illustrated in Figure 43 where the device response is shown for 3 ns pulses of 100, 200, 300, 400 and 500 V. As is clearly evident, the device remains in its high impedance state for pulse voltages of at least 400 V and thus any circuit in parallel with this device will under these conditions, experience the full pulse voltage. When the pulse voltage is further increased to 500 V, the device switches to its low impedance state, in less than 1 ns, and the maximum voltage observed, the threshold switching voltage, is ~ 200 V (when account is also taken of inductive effects). It is very important to recognize in applications which use this device that circuit protection may not be obtained even for input voltage pulses considerably in excess of the threshold switching voltage as measured and described in this report. The device must switch before circuit protection for voltages of value V_{th} is achieved.

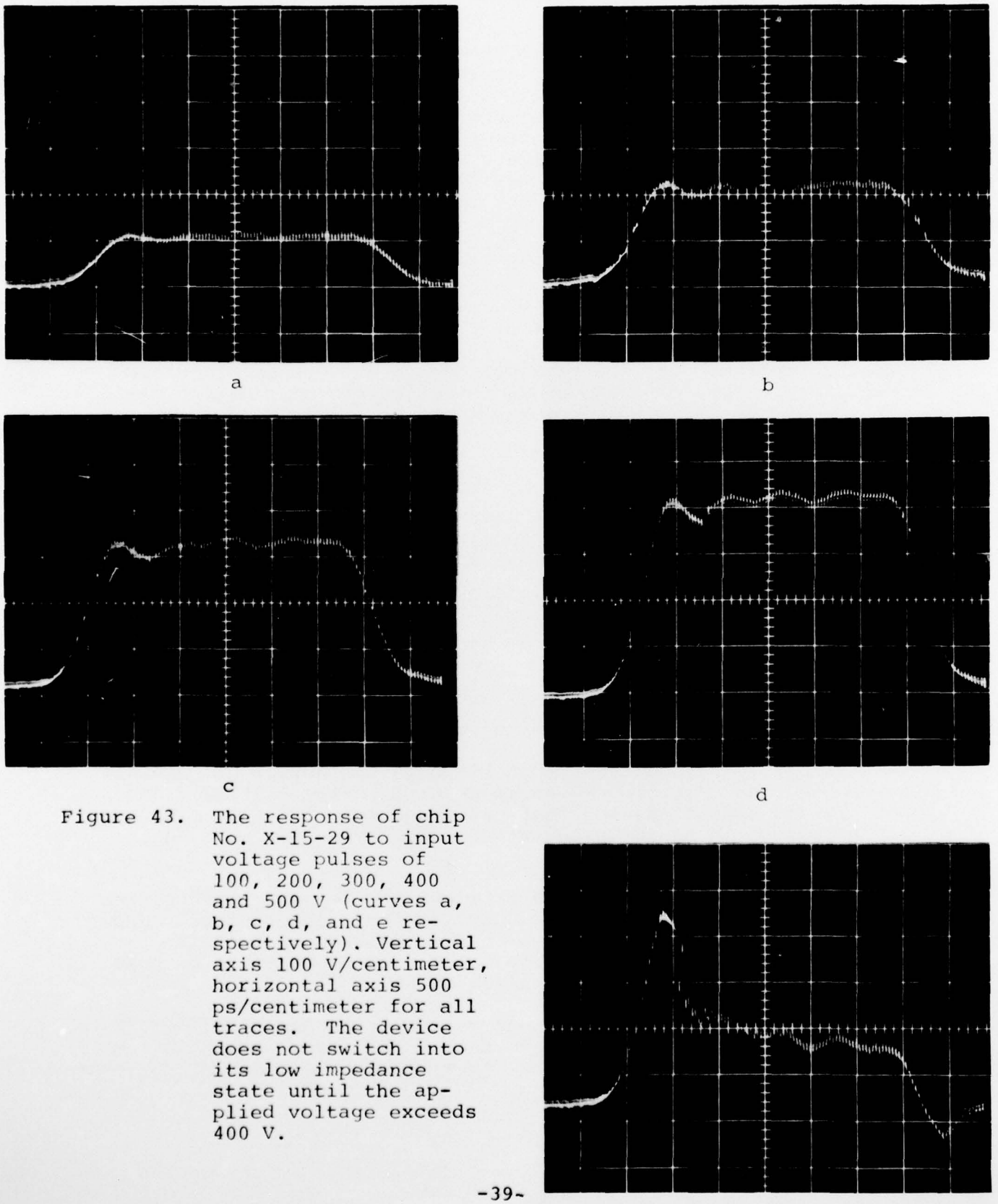


Figure 43. The response of chip No. X-15-29 to input voltage pulses of 100, 200, 300, 400 and 500 V (curves a, b, c, d, and e respectively). Vertical axis 100 V/centimeter, horizontal axis 500 ps/centimeter for all traces. The device does not switch into its low impedance state until the applied voltage exceeds 400 V.

XV. CONCLUSIONS

The primary conclusions to date are as follows: The NbO/NbO_2 chips supplied by ECOM do exhibit switching with a delay time of less than 1 ns. The electrical parameters of these chips do not however meet the specifications listed in the Technical Guidelines DAAB07-76-Q-1335. The threshold switching voltage is typically 100-300 V and not <100 V as specified. Switching characteristics and off state resistance are highly variable between chips and even from place to place on a single chip. Device degradation with repeated pulsing is observable for 3 ns pulse width and degradation is markedly accelerated for larger pulse widths. Samples subjected to long (50 ns) pulses or extensive pulsing (thousands of 3 ns pulses) exhibit deep channels through the NbO_2 layer to the NbO substrate. Samples with less severe pulsing show less physical damage, but deterioration is sometimes observed in device off state resistance. There is no clear correlation between physical damage and device off state resistance. The switching characteristics and degradation with pulsing of the devices do not appear to be a function of the electrode material.

XVI. RECOMMENDATIONS

Coaxial switching devices made from the chips supplied by ECOM (physically described in Section II) do not fulfill requirements for NEMP protective devices as described in the Detailed Requirements Section (3.2.1 to 3.2.10) of the Technical Guidelines DAAB07-76-Q-1335. It is stated therein that the device must have sufficiently high impedance in the off state to ensure minimum insertion loss (less than 0.4 dB at 200 MHz) while in the on state the device voltage should never exceed 100 V with a corresponding delay time of less than 1 ns, and in addition, should withstand 1000 switching cycles of 100A for 1 ms or 20 A for 5 ms without suffering a significant change in protection capabilities.

It was found, however, that although the device did exhibit switching, the switching voltages were typically 100-300 V and not <100 as specified, and that device degradation took place for pulses of 50 ns duration and even for extensive pulsing in the 3 ns range.

If the NbO_2 layers of the ECOM chips were made thinner, the switching threshold could be reduced to the required level. However, a device made from such a chip might show an increased insertion loss and most probably would degrade even faster than one fabricated from the as supplied chips.

If the Detailed Requirements set forth in DAAB07-76-Q-1335 are firm, then it is recommended that alternative work plans be initiated which show better prospects of meeting the NEMP requirements.

Basic studies of the mechanisms of switching in materials such as NbO_2 should be made. In parallel with such studies, an empirical approach could be taken in which "good guesses" are made concerning those factors which may influence device performance and stability. Recommended areas for future investigation are outlined below.

1. Evaluate single crystal niobium oxide materials.

2. Evaluate NbO/NbO_2 chips in which the grain size and structure of the NbO_2 layer is altered by changes in the oxidation procedures.

3. Evaluate NbO/NbO_2 chips for a range of added oxide stoichiometry.

4. Evaluate NbO/NbO_2 chips which utilize buried contacts (for example, In diffusion in NbO_2 layer). This may affect surface deterioration and hence device stability.

5. Evaluate other types of devices (metal oxide varistors, silicon controlled rectifiers, etc.) for possible use in NEMP devices.

Of these areas, 1 and possibly 2 could be addressed within the time and funding constraints of the present contract.

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